09852860 '082691

FIG. 1

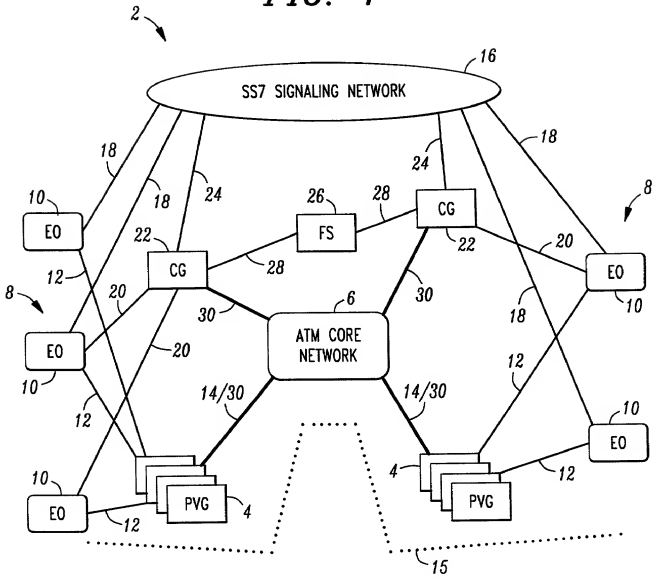


FIG. 2

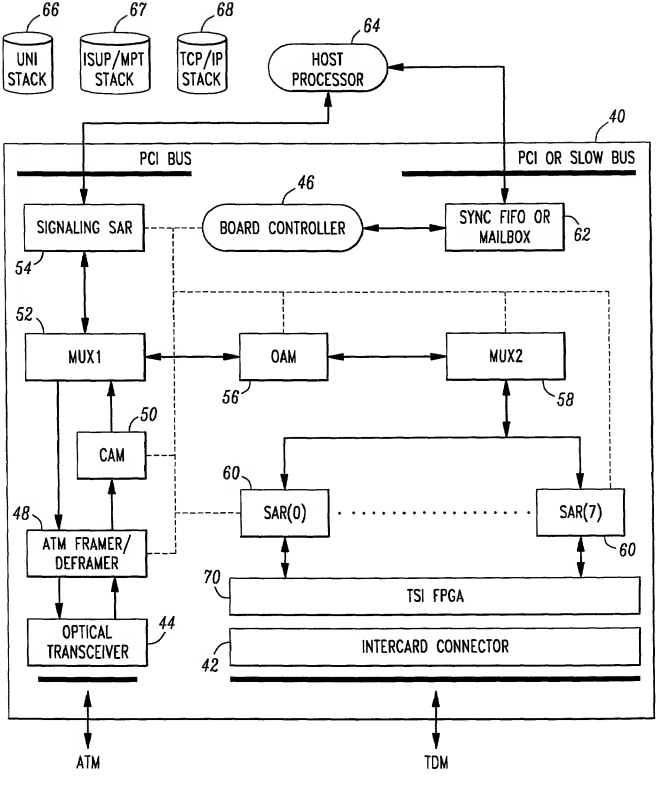
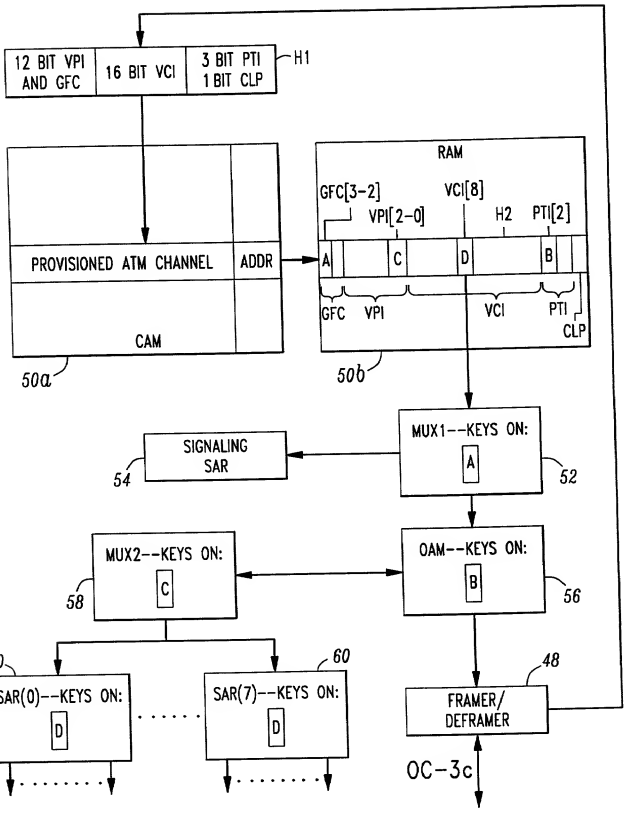

66
67
68
64
UNI STACK
ISUP/MPT STACK
TCP/IP STACK
HOST PROCESSOR
40
PCI BUS
PCI OR SLOW BUS
46
SIGNALING SAR
BOARD CONTROLLER
SYNC FIFO OR MAILBOX
62
54
52
MUX1
OAM
MUX2
56
58
50
CAM
60
48
SAR(0)
SAR(7)
ATM FRAMER/ DEFRAMER
60
70
TSI FPGA
OPTICAL TRANSCEIVER
44
INTERCARD CONNECTOR
42
ATM
TDM

FIG. 3


12 BIT VPI AND GFC
16 BIT VCI
3 BIT PTI 1 BIT CLP
H1
PROVISIONED ATM CHANNEL
ADDR
CAM
50a
RAM
GFC[3-2]
VPI[2-0]
VCI[8]
H2
PTI[2]
A
C
D
B
GFC
VPI
VCI
PTI
CLP
50b
MUX1--KEYS ON:
A
52
SIGNALING SAR
54
MUX2--KEYS ON:
C
58
OAM--KEYS ON:
B
56
60
SAR(0)--KEYS ON:
D
SAR(7)--KEYS ON:
D
60
48
FRAMER/ DEFRAMER
OC-3c

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HEADER FIELD	GFC 4-BIT		VPI 8-BIT		VCI 16-BIT			PTI 3-BIT		CLP	MUX1	OAM	MUX2	SAR
BIT FIELD POSITION	3-2 (A)	1-0	7-3	2-0 (C)	15-9	8 (D)	7-0	2 (B)	1-0	0	KEY ON GFC[3-2]	KEY ON PTI[2]	KEY ON VPI[2-0]	KEY ON VCI[8]
AAL1 USER CELLS	0	X	X	ANY	X	1	ANY	0	X	X	1-TO-4 DEMUX TO OAM	USER CELLS 0 PASS-THROUGH	1-TO-8 DEMUX	256 DSO CHANNELS
SEG/END F5 OAM CELLS	0	X	X	=USER	X	1	SAME AS =USER	1	X	X	SAME AS ABOVE	OAM F5 CELLS ARE TERMINATED	N/A	N/A
SEG/END F4 OAM CELLS	0	X	ANY	ANY	X	0	SEG=3, END-TO-END=4	1	X	X	SAME AS ABOVE	OAM VCI=3 OR 4 ARE TERMINATED	N/A	N/A
SIGNALING HAIRPIN	0	X	ANY	ANY	X	0	ANY	0	X	X	SAME AS ABOVE	PASS THROUGH	1-TO-8 DEMUX	OAM QUEUE
UNHANDLED F5 OAM CELLS	0	X	X	=USER	0	1	SAME AS =USER	0	X	X	SAME AS ABOVE	PASS THROUGH	1-TO-8 DEMUX	OAM QUEUE
UNHANDLED F4 OAM CELLS	0	X	ANY	ANY	X	0	SEG=3, END-TO-END=4	0	X	X	SAME AS ABOVE	PASS THROUGH	1-TO-8 DEMUX	OAM QUEUE
AAL5 DATA CELLS	1	ANY	ANY	ANY	ANY	A	ANY	0	X	X	1-TO-4 DEMUX TO SIGNALING SAR	N/A	N/A	N/A
AAL5 F5 OAM CELLS	1	SAME AS AAL5 DATA CELLS						1	X	X	SAME AS ABOVE	N/A	N/A	N/A
AAL5 F4 OAM CELLS	1	ANY	ANY	ANY	ANY	0	SEG=3, END-TO-END=4	X	X	X	SAME AS ABOVE	N/A	N/A	N/A

FIG. 4

FIG. 5

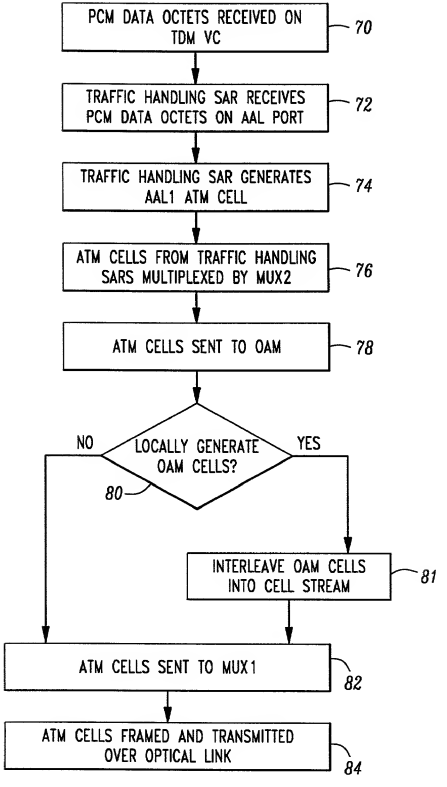

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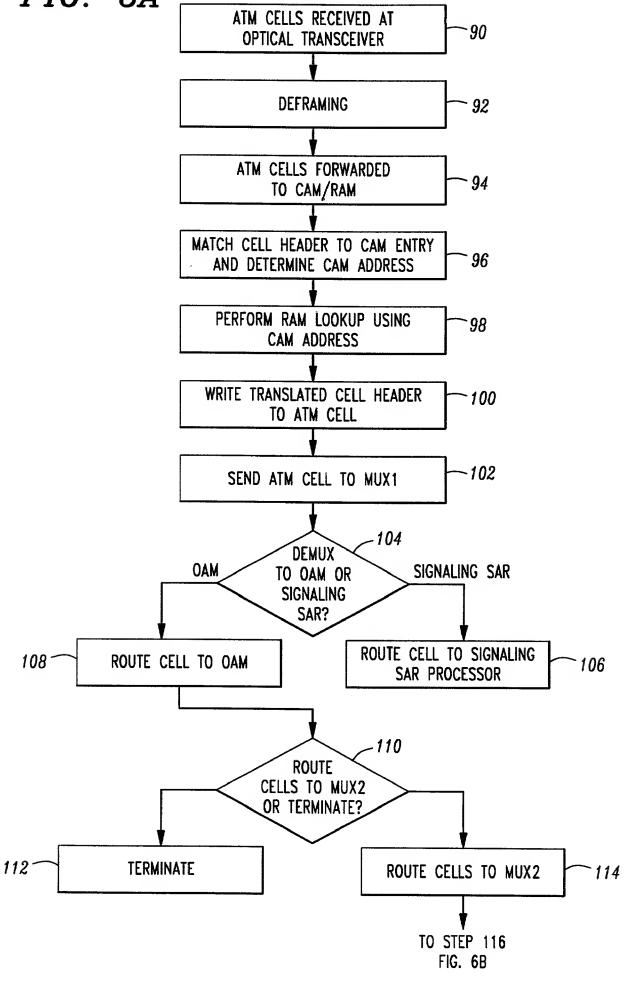
FIG. 6A



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09/680,765
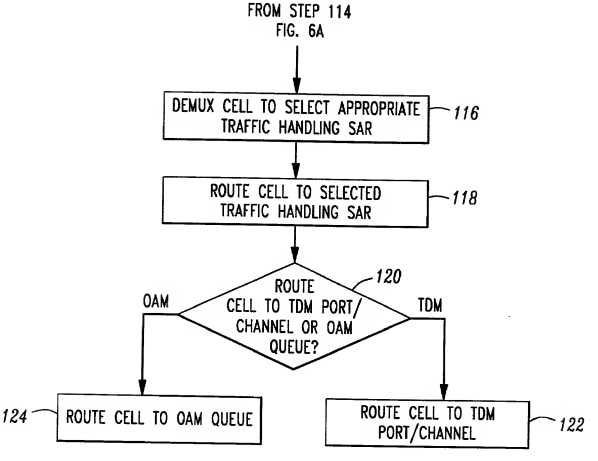
FIG. 6B